

Review Article

Controlled Crystal-Growth and Structures of Silicon Nanowires for Smart Applications.Maha Mohammed Khayyat ¹, Brahim Aïssa ^{2,3,*}, Esam H. Abdul-Hafidh ⁴, Mourad Nedil ⁵

1. Physics department of Umm al-Qura University (UQU), P.O. Box 715, Makkah Al-Mukaramah 21955, Kingdom of Saudi Arabia. Email: maha.khayyat@gmail.com
2. Qatar Environment & Energy Research Institute (QEERI), Hamad Bin Khalifa University (HBKU), Qatar-Foundation. P.O. Box 5825, Doha, Qatar. Emails: baissa@qf.org.qa
3. College of Science and Engineering (CSE), Hamad Bin Khalifa University (HBKU), Qatar-Foundation, P.O. Box 5825, education city, Doha, Qatar.
4. Physics department. Yanbu University College. P.O. Box 31387, KSA. Email: essama@yuc.edu.sa
5. Telebec Wireless Underground Communication Laboratory, UQAT, 675, 1^{ère} Avenue, Val d'Or, Québec, J9P 1Y3, Canada. Email: mourad.nedil@uqat.ca

*E-mail: baissa@qf.org.qa

Received date: 14-11-2015; Accepted date: 06-12-2015; Published date: 09-12-2015

Abstract: One-dimensional nanostructures such as semiconductor nanowires (NWs) are attractive building blocks due to their promising physical properties and potential as active materials in future electronic and optoelectronic applications. The Crystal growth of nanowires occurs mainly at the interfaces between the growing crystals and the supply media. This article reports on the silicon nanowires grown using a vapor-liquid-solid (VLS) concept. One of the key advantages and the beauty of VLS is that controlled placement or templating of the seed metal produces consequently templated NW growth. This templating is highly required for direct integration of NWs into nanodevices for various smart applications, including sensors, actuators, thermoelectricity generation and photovoltaics. We discuss the major questions related to the discovery of fundamentally new phenomena versus performance benchmarking for many of the Si-NWs applications. Finally we attempt to look into the future and discuss our opinion regarding the upcoming trends in NW research.

Key words: Silicon nanowires. Crystal Growth. Smart applications. Innovation. Engineering.

Corresponding author: Brahim Aïssa

Address: Qatar Environment & Energy Research Institute (QEERI), Hamad Bin Khalifa University (HBKU), Qatar-Foundation. P.O. Box 5825, Doha, Qatar

Introduction

Silicon nanowires (Si-NWs) represent a particularly attractive class of building blocks for nanoelectronics because their diameter and electronic properties can be controlled during synthesis in a predictable manner. They have recently attracted much more attention due to the historical role of Si in devices fabrication and in the integrated circuits (IC) industry. Continued high performance from Si may require integration of innovative architectures of NWs with the exciting functional devices. Si-NWs may provide new avenues in these directions. Recently, Si-NWs have been used in the fabrication of DNA sensors [1]. The ability to control the

unique morphological and mechanical properties of Si-NWs arrays demonstrated by Paulo and coworkers [2] opens new perspectives for the development of array based electrical and electrochemical systems. In addition, there are studies [3,4] of fabricating Si-NWs vertical surround-gate field effect transistor (VS-FET). It has been reported [5] that room temperature electroluminescence has been appeared from undoped Si-NWs that were grown from disilane at a wavelength excitation of 600 nm. It has been as well shown recently that Si-NWs have been used to produce high resolution Atomic Force Microscope (AFM) [6].

Device applications utilizing Si-NWs have been demonstrated in many different applications including optoelectronic and electrical devices, as well as solar cells [7-10]. This article reports on the wires grown using a vapor-liquid-solid (VLS) concept and similar three phases processes [11-14]. One of the key advantages of the VLS process is that the controlled placement or templating of the seed metal produces templated NW growth. This templating is required for the straightforward integration of NWs with other devices which is desirable for many applications. Templated growth of NWs have been achieved using various noble metals like Au, Ag and Cu as the seed sites [15-18] but for more reactive metals like Al, Sn and Sb templating has often proven difficult. The noble metals can often negatively affect the semiconductor properties of the nanowire from an application perspective [12,13,15,19-22]. For example Au is a deep level trap in Si. Whereas the more reactive metals like Al, Sb, and Sn are less parasitic and can even be positive in terms of acting as desirable dopants when incorporated in the semiconductors [23-25]. Controlling spatial placement of VLS grown nanowires with oxygen reactive seed metals is therefore of great interest for nanotechnology based applications [26].

It is our intent to describe in general the growth of Si-NWs in a three phases system. Therefore general terms describing the three phases of the system to be used throughout this article will first be defined. In this work, the term supply is used to indicate the phase that supplies the growth species to the surfaces. Common supply media are vapors, solutions, melts, or even molecular beams through vacuums. The term crystal or wire, as defined above, will be used to describe the solid crystalline phase. The term collector is used to describe the third phase, which is small in comparison to the vapor crystal interface. This term is used to replace more specific terms like: liquid droplet, crystalline particle, catalysts, etc. The 1-D crystal growth occurs at the interface between the collector and the wire with the collector either at the base or on the tip of the wire, (a schematic is described in figure 2). Unlike conventional crystal growth with only two components or phases nanowires are often grown in a three phase system. The vapor-liquid-solid (VLS) growth mechanism describes such a three-phase system where the third phase is also important to the crystal growth. This or similar growth mechanisms are currently the accepted mechanism for the enhancement of the epitaxial growth of most free standing wire-like crystals [10,15,27]. The VLS mechanism is based on a specific system there are three components; a vapor which supplies the source materials for crystal growth, a liquid droplet, and the solid crystal. In order for 1-D growth to result from this three-phase system, the surface area of the liquid phase must be physically small in comparison to the surface area of the vapor/crystal interface. One-dimensional crystal growth results when the growth rates at the phase boundary between the liquid phase and the solid crystal surface is higher than the growth rate at the

vapor/solid phase boundary. The commonality being that there are three phases and the VLS mechanism is used as a basis to say that the existence of three phases is sufficient explanation of the growth mechanism. Some examples are the vapor-solid-solid (VSS), [28-30] vapor-adsorption layer-solid (VAdS), [28] solid-liquid-solid (SLS), solution-liquid-solid (SLS) and supercritical-fluid-solid or liquid-solid (SFSS or SFLS) growth processes, [31,32]. The VLS growth mechanism is therefore examined in order to reveal the atomistic processes involved in crystal growth in a three-phase system.

On the other hand, the number of publications dealing with various aspects of silicon nanowires has increased markedly in recent years as depicted in Figure 1. Along with the increase in the number of publications and late advances in this area, raises a need for this executive review, and one of the objectives of this article is indeed to address this need.

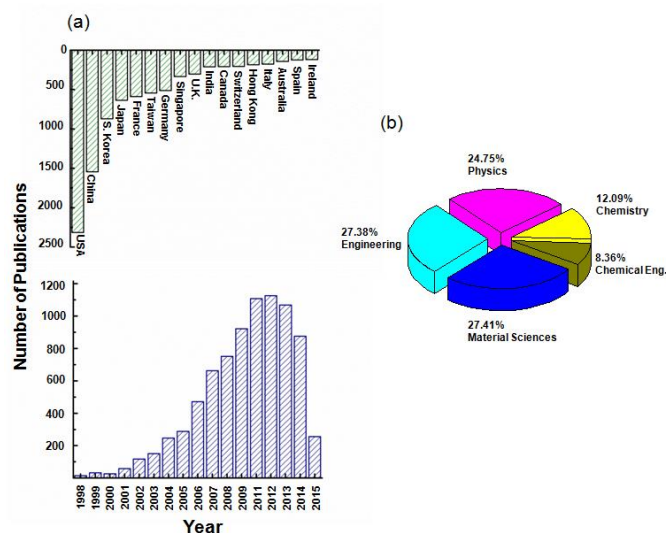


Figure 1: (a) Recent refereed publications related to the field of silicon nanowires, together with their corresponding distribution of subject area and distribution countries. All published languages were included. All document types, including journal and conference articles, report review, conference proceeding, and monograph published chapters were recorded. Statistics are available from 2000 to august 2015 inclusively. Data were collected from Scopus of peer-reviewed literature web based information service.

Aspects of Synthesis

Investigation of Si-NWs or Si whiskers dates back to the pioneering work on vapor-liquid-solid (VLS) approach by Wagner and Ellis [33, 34]. The key to NWs growth in any three phase system is that the nucleation and growth rate at the collector/crystal (liquid/solid) interface is greater than the growth rate at the supply/crystal (vapor/solid) interface. This means that the crystal grows more rapidly under the collector, forming a nanowire with approximately the same diameter as the collector. The aspect ratio of the nanowire is

dependent on the selectivity of the growth rates at the different collector/crystal and supply/crystal interfaces. The Si-NWs grown via VLS reaction are single crystals but exhibit growth defects such as bending and kinking. Lowering the silane (SiH_4) partial pressure leads to an increase in the wire width and a reduction in the tendency to form kinks. The VLS reaction using silane as the Si source gas allows the growth of the very thin wires with high aspect ratio [17,18].

There are three main production schemes for forming nanowires. In the top-down approach, lithography or some other means is used to pattern a planar substrate material. An anisotropic etch is then used to remove the material between the nanowires. In the bottom-up approach, either a seed particle or a patterned surface is used to define where the nanowires will grow. Physical or chemical vapor deposition (CVD) methods are then used to supply growth precursors which feed the growth of crystalline nanowires. Nanowires can also be produced by forming the crystalline nanostructures from an amorphous material.

A summary of the VLS growth process steps of Si-NWs catalyzed for instance with Au is shown in **figure 2**. Similar process can be applied to grow Si-NWs seeded with Al collector particles over a relatively wide process window.

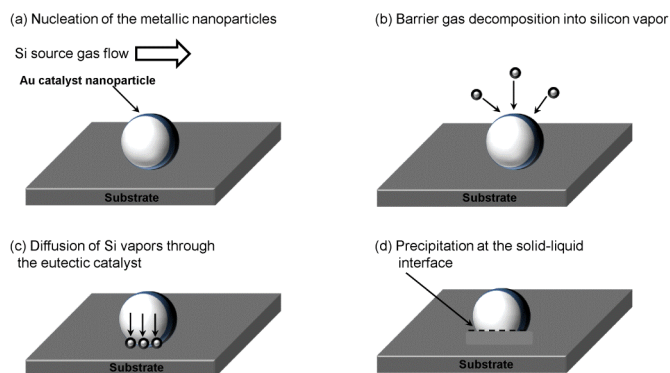


Figure 2: Schematic representation of growth steps of VLS-assisted growth of Si-NWs. Adapted from [35].

Systematic changes in the nanowire morphology have been identified with respect to the Al film thickness, growth temperature, and pressure. The Si-NWs can be grown with high growth rates, good morphology, i.e., epitaxially with low diameter dispersion and tapering), and at high density over a large range of growth conditions [12,13]. In fact, from our experience growing nanowires with both Au and Al we have found that it is simpler to achieve high densities, low diameter dispersion, and good alignment with Al than it is with Au. However, the key to good growth with Al is careful deposition and treatment of the Al layer prior to growth, particularly with respect to avoiding oxidation; dramatic changes in the results can be attributed to small changes in the base pressure used to deposit the Al films. Post growth and in-situ studies with varied thermal treatment of the Al film allow the state of the collector to be probed and suggest that the collector is an under cooled liquid during growth. This

understanding may be important in forming more complex nanowire-based structures in this materials system, particularly in terms of the pre-growth conditions. We also confirmed that Al is incorporated in the nanowires during growth as an active dopant and as a species that can later be activated by high temperature treatment of the nanowires. The incorporation levels are higher than the projected bulk solid solubility, which could lead one to conclude that if this high incorporation is possible with Al it is also possible when growing nanowires with other metals. The structure and electronic characteristics of these Al grown Si wires are highly relevant to many applications, for example, in photovoltaics, where it is advantageous to eliminate Au, where p-type doping is helpful in forming the structures, and where novel faceted structures like the pyramidal structure presented here may be useful in terms of multiple internal scattering of photons to increase efficiency.

Catalyst Choice

The metal nanoparticle has a major role in vapor-liquid-solid assisted nanowire growth. The metal particle plays the act of the catalyst and determines the diameter of the nanostructures. Consequently, the choice of the metal, based on its physical and chemical properties, determines many of the nanowires properties. To be processed via the VLS growth mechanism, the metal has to be physically active, but chemically stable. To find an eligible metal, the phase diagram is first consulted to choose a material that forms a liquid alloy with the nanowire material of interest. The phase diagram is also helpful for estimating the optimal composition and temperature for nanowire growth.

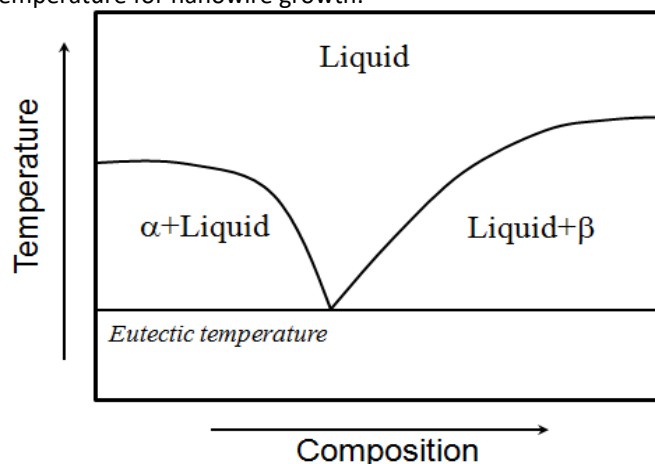


Figure 3: Binary phase diagram of alloy suitable for VLS mechanism.

In the vapor-liquid-solid process, the Gibbs-Thomson equation places a lower limit on the wire diameters that can be achieved under a given set of conditions. Givargizov [36] has studied also in detail the VLS crystal growth technique in 1975, according to his study the equilibrium state is given by the following equation;

$\Delta\mu_{NW} = \Delta\mu_B - 4\frac{\Omega\alpha}{d}$	Equation 1
$\Delta\mu_B = \mu_B - \mu_V$	Equation 2
$\Delta\mu_{NW} = \mu_{NW} - \mu_V$	Equation 3

Where μ_{NW}, μ_B, μ_V are the effective chemical potentials of silicon in the nanowire, in the bulk material, and in the vapor phase respectively, d is the diameter of the nanowire, Ω is the atomic volume of silicon, and α is the specific surface free energy of the wire.

There is a critical nanowire diameter at which the growth stops completely, the relation is as follows;

$\frac{\Delta\mu_B}{kT} = \frac{4\Omega\alpha}{kT d_c}$	Equation 4
---	------------

Where k is the Boltzman's constant and T the temperature, d_c the critical diameter.

Interestingly, the VLS growth is not actually a catalytic process and the seed metal is not really a catalyst. The metal droplet just receives the source material and when supersaturation is reached, the excess material precipitates out of the droplet in the form of a NW. Thus, the seed metal is only a "soft template" [37, 38] to collect the material and facilitate NW precipitation, guidance, and elongation in the axial direction.

A catalyst, as well known in chemistry literature and chemical industry, is a material that increases the rate of a chemical reaction while remaining intact in the process. The activation energy for Si-NW growth using Au seeds and Si thin film growth in microelectronics industry is about the same at about 130 kJ/mol [38], indicating that Au does not aid in increasing the reaction rate.

Au is the most favored seed metal in the literature for NW growth due to the ease of handle. However, Au is viewed as a contaminant in semiconductor processing. It can modulate carrier recombination in both n-type and p-type materials because high-mobility interstitial Au atoms can transform into electrically active low-mobility substitutional sites. Gold is not desirable also in optoelectronics applications since, as a deep level trap in Si, it causes fast non radiative decay of excited carriers. For this reason, Si-NWs with Au catalyst are not capable of light emission whereas the NWs produced with other seed metals or oxide-assisted growth is known to produce light emission in the visible and near IR ranges. Another disadvantage is the high eutectic composition of Au-Si system at 371 °C (31 atm. % of Si), which would make it impossible to obtain abrupt heterojunctions in a NW by rapidly switching the gas phase precursors.

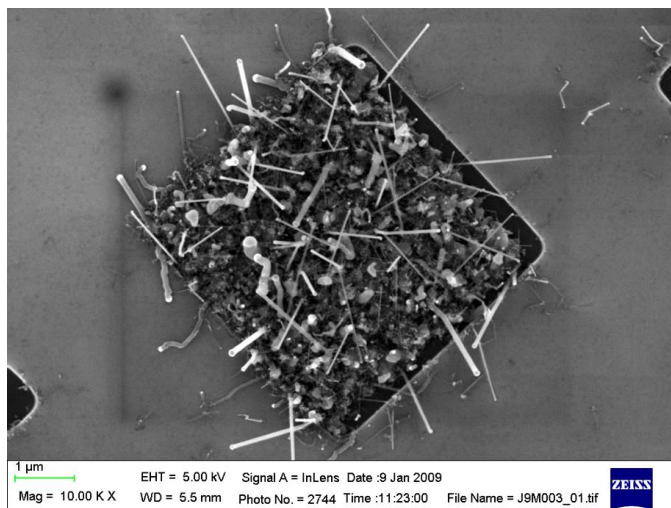


Figure 4: Si-NWs catalyzed with Au, patterned growth using photolithography. Experiments were carried out by one of the authors (Maha Khayyat) in 2009 at T. J. Watson Research Center.

For these reasons, several alternatives to Au have been investigated in Si-NW [39]. Gallium is a metal with low melting point which forms a eutectic at a low temperature (29.8 °C) with low Si content (only 5×10^{-8} atm. %). $TiSi_2$ has been successfully used as a catalyst for Si-NW growth [40]. Titanium sputtered onto a silicon wafer forms small islands of $TiSi_2$ when annealed at 900 °C in hydrogen for 5 min. Similarly, a thin layer of Pt on Si wafer obtained by physical vapor deposition forms PtSi when annealed at high temperatures. PtSi commonly used as interconnects, has also been used in Si-NW growth [41].

Templated Si-NWs seeded with Au using standard photolithography is shown in figure 4 on Si (100) substrate. The carried out the work presented in figure 4 as a starting point to catalyze the growth of Si-NWs, as it is a well-established material. The knowledge of parameters determine the diameter of Si-NWs using Au as a collector was used to grow Si-NWs using Al. The interest in other metals for Si-NWs has arisen from the fact that Au historically has poor compatibility with Si devices because Au impurities act as a deep level trap decreasing the carrier mobility, lifetime, and diffusion length. The cost and the availability of Au is especially important for photovoltaic applications, leading to recent efforts using Al and other non-gold metal for NWs growth of photovoltaic Si structures based on nanowires.

Nanoscale Chemical Templating (NCT) using oxygen reactive materials

Why we need to control the growth place of NWs? Applications for NWs grown using the VLS process have been demonstrated in many optoelectronic and electronic devices. In order to broaden this application space and make NW based devices commercially viable, control of the placement or templating of the nanowires is desired. Templating is well

established using noble metals like Au, Ag and Cu, but for more reactive metals like Al, Sn and Sb templating has been difficult. Array of vertically aligned Si-NWs were grown over areas $>1 \text{ cm}^2$ by standard photolithography [16]. This is because when the seed metal reacts with oxygen or oxygen containing materials prior to the growth, the VLS process is hence impeded. Here we describe an innovative process that we call “nanoscale chemical templating” (NCT) which takes advantage of the reactivity of the seed metal to template the NW growth. NCT uses oxygen containing mask layer like SiO_2 to prevent the growth of NWs in undesired locations. In the desired growth locations the mask is removed prior to metal deposition so that NWs can grow in the holes in the oxide mask. NCT can have a selectivity of 100 %, meaning that where there is oxide NWs do not grow. The growth yield depends on the processing parameters and mask dimensions. High yields of single vertically aligned NWs per sight are possible. Preliminary optimization was found to produce a 76 % yield of single wires and 97 % yield per mask opening. Most of the excess yield is multiple vertically aligned wires per sight.

Most of the conventional NW templating techniques do not work with oxygen reactive seed materials like Al. The reason is that they require liquid based chemistries that would oxidize reactive materials rendering the entire layer inactive for seeding NW growth. In a typical templating process consists of the following five steps:

- (i) A mask with holes through to the substrate where NW growth is desired is formed;
- (ii) A metal is blanket layer is deposited over the mask;
- (iii) The substrate with the over-layer is annealed and the Au reacts with the substrate in the holes and forms the NW seeds;
- (iv) A liftoff of the metal is performed by removing the mask;
- (v) NWs are grown.

Depending on the mask the order of step (iii) and (iv) can be reversed. When the order kept as stated the mask, such as a SiO_2 mask, can prevent surface migration of metal during the annealing process. If liftoff is performed first, metal migration during annealing can become a problem for pattern fidelity. If the metal is not removed from the areas above mask, NWs will grow in disordered crystallographic directions on top of the amorphous mask. Thus for a typical templated growth process with high fidelity a liftoff process is required after the annealing of the seed material with the substrate.

NCT starts with the same processes as conventional NW templating (see figures 2a-c).

(i) Forming a mask with holes where NW growth is desired. The only constraint here is that this mask must be a material that will chemically react with the desired seed material and render it unsuitable as a NW seed. The second step (ii) a blanket deposition of the seed material is also the same. In NCT this layer must however be protected from oxidation. In this paper this is achieved by depositing the metal layer in the

load lock chamber of the ultra high vacuum- chemical vapor deposition (UHV-CVD) system and not exposing the deposited layer to air before the next steps (iii) annealing and (iv) growth.

It is believed that another method for preserving this layer would be to deposit an amorphous layer of the desired nanowire material over the non-oxidized metal layer. This layer will protect the seed layer from oxidation but still allow NW growth. In NCT the metal layer does not require additional patterning processes like lift off but is only deposited as a blanket and annealed. This seed layer could be removed after NW growth by selective etching of the oxidized metal, or it can remain as an isolation layer between the NWs. In fact liftoff is one of the liquid based processes that would oxidize the entire reactive seed layer preventing NW growth.

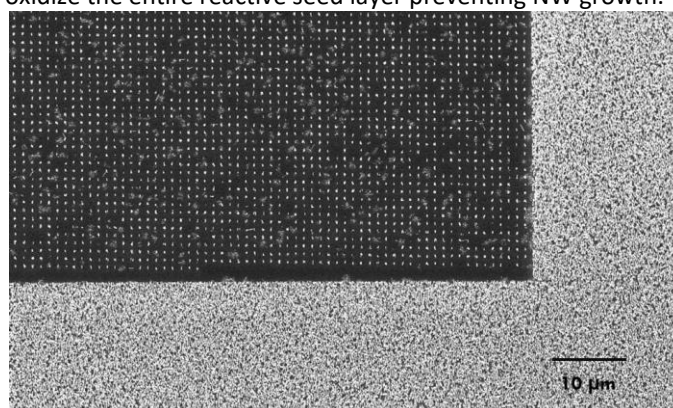


Figure 5: Scanning Electron Microscopy (SEM) micrograph showing patterned and un-patterned growth of NWs on Si (111) substrate.

The Si (111) sample, which has opening between a SiO_2 layer of 50 nm thickness, was placed in the load lock of a custom built ultra-high vacuum chemical vapor deposition (UHV-CVD) tool operated under low pressure conditions (LPCVD). Then Al layer of 6 nm thickness was thermally evaporated on the oxide patterned Si (111) sample, where the Al evaporator and a quartz crystal monitor were installed in the load lock. The load lock base pressure was maintained in the range 10^{-7} Torr and the growth chamber has a base pressure of 10^{-8} Torr, at 600 °C. Then the sample was transferred to the hot growth chamber to be annealed at 750 °C, for 20 minutes. The annealing temperature is higher than the eutectic temperature (577 °C as pointed by Givargizov [36]) to agglomerate into relatively large islands on the opening. Then the furnace was cooled below the eutectic temperature then the silane (SiH_4) was introduced at a fixed flow rate of 10 sccm (standard cubic centimeter per minute), along with the diborane (B_2H_6) with a flow rate of 1 sccm. The growth time and pressure were 60 minutes 550 mTorr, respectively. After NWs growth the SiH_4 and B_2H_4 were pumped out, and then the samples were transferred to the load lock and allowed to cool down for few minutes. The NWs morphology was studied by scanning electron microscopy.

Figure 4 shows a SEM image of patterned growth using NCT along with zones showing non-patterned growth of Si-NWs.

To demonstrate the versatility of NCT we have used patterns produced with both photolithography and nanosphere lithography. The type of photolithography used is not thought to be an important parameter in NCT. In order to produce single NW per opening, holes on the order of 200 nm were required. This was achievable by the deep UV lithography, but could have been performed by e-beam lithography or nano-imprint lithography. The photolithography substrates were 200 mm p-type (111) Si wafers which were processed by first growing a 50 nm thick layer of SiO₂ at 950 °C in a standard oxide growth process. This oxide layer was then patterned with a 90 nm thick anti-reflection coating (ARC) followed by 450 nm thick photoresist (UV1 1 0G) using a 248 nm ASML UV- excimer laser stepper to expose the pattern. The purpose behind using an ARC coating is to primarily to reduce the light reflection and furthermore to increase the total PV efficiency for the elaborated solar cell devices. The pattern consisted of circular holes with a center to center spacing of 1.95 μm and a nominal diameter of 200 nm. After development of the resist and ARC open/resist trim by reactive ion etching in N₂/O₂, the wafers were subsequently broken up into samples of approximately 1 cm² for further individual processing.

The pattern in the resist was transferred into the oxide by etching the oxide with buffered HF (BOE 9:1 Seidler Chemical Company) solution, typically for 60 s. The photoresist and ARC were removed from the remaining area with acetone followed by IPA and finally by an O₂ ash treatment (100 W, 15 sccm, ≤1 Torr). This produced 233 ± 5 nm openings in the 50 nm oxide, varying the buffered HF. Directly before loading the substrate into the load lock of the UHV-CVD chamber the samples were treated again in the buffered HF for 4 seconds to remove residual oxides that were formed during processing and storage. The etch time was tuned to completely clear the oxide from the openings without expanding the openings. The UHV-CVD load lock chamber has been modified with capabilities for Al evaporation, and after pumping the chamber to below 10⁻⁶ Torr, 6 nm Al was deposited as described previously. The sample was then annealed at 730 °C for 10 minutes. This annealing temperature is higher than the eutectic temperature (577 ± 1 °C) for Si and Al, the Al deposited on clean Si as in the mask openings reacts with the Si substrate to form Si:Al eutectic droplets from which nanowires can subsequently grow. However, thin Al deposited on the SiO₂ does not produce NWs.

After annealing, the growth of nanowires was carried out by cooling the furnace to the desired growth temperature at 490 °C. Pure silane was introduced at a fixed flow rate of 10 sccm, along with a diborane helium gas mixture (B₂H₆: He = 1:1000) with a flow rate of 1 sccm. A schematic flow of NCT is

included in **figure 6**, in addition to scanning electron microscopy (SEM) micrographs of experiments we conducted.

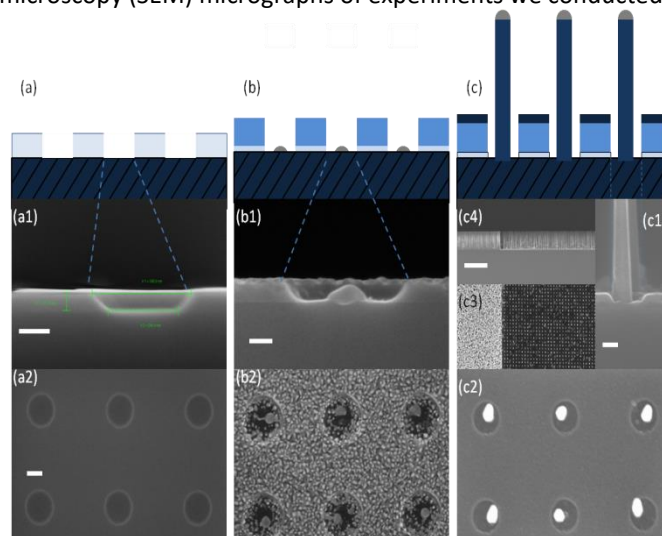


Figure 6: (a-c) Illustration of NCT of NWs, and corresponding SEM images, cross sectional (a₁ to c₄) and top views (a₂-c₃).

The substrates for nanosphere lithography were pieces of a p-type (111) Si wafers ~ 2 cm² which are cleaned using standard techniques, leaving a thin oxide on after cleaning. Silica microspheres are commercially available with narrow size distributions, and when dispersed properly on a surface they can form a close-packed array that defines gaps through which a NW seed material can be deposited. In our case a drop of Silica microspheres solution taken directly from the bottle was dispersed onto the substrate. Variable speed spin routines were used on a resist spinner to remove the liquid and disperse the particles. After spinning on the microspheres the substrates were processed like the photolithography samples after the resist strip. Namely they were cleaned with O₂ plasma, etched with HF, inserted into the load lock, and Al was deposited. In **figure 6a₁**) and **b₁**) a NCT scheme using microspheres is illustrated. In this scheme an Al seed layer forms at the gaps between microspheres and on top of the microspheres the Al layer reacts with the oxides in the spheres. Al deposition, annealing, and NW growth were performed under the same conditions as with the photolithography samples.

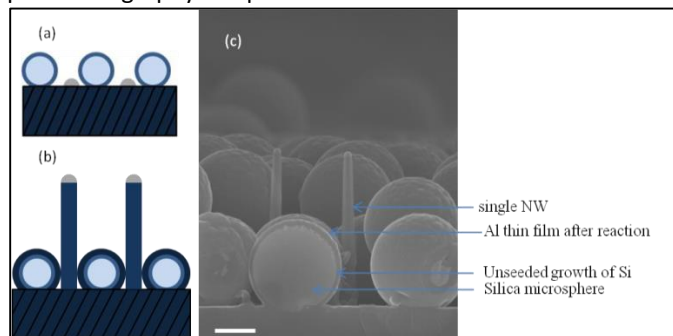


Figure 7: Schematic representation of the use of NCT with silica microspheres. (a) The microspheres dispersed on a Si substrate. (b) After Al deposition and heating. (c) On exposure to silane. (d) A cross sectional SEM image showing single NW growth between microspheres. Note the darker contrast at the microsphere surface due to unseeded Si growth and the brighter line at the interface where the Al was deposited. (The scale bar is 500 nm).

In both conventional nanowires templating and NCT advantages appropriate mask, deposition, and annealing processing conditions can be found that form well-defined NW seeds. These seeds control the growth of the NWs with no NW growth occurring between mask openings. Also depending on the width of the opening, it is possible to grow a plurality of NWs or a single NW within each opening. The advantages of choosing NCT with an oxygen reactive material like Al as the seed material for Si nanowires rather than conventional templating with Au are:

- (a) The fundamental problem of low lifetime due to deep level traps caused by incorporation of Au into the Si can be avoided;
- (b) Al provides lightly p-doped Si NWs, so that p doped nanowires can be grown without the morphological changes in NWs which typically occur during in situ doping by B₂H₆ are avoided;
- (c) The reaction of Al with the SiO₂ mask during an initial anneal avoids the need for removing the unwanted seed material by lift off. No NWs grow between the desired spots even when the seed material is not removed. This simplifies the processing by requiring fewer processing steps;
- (d) Al remaining post-growth at the tips of the NWs can easily be removed by a simple HF treatment. To remove Au from the tips more exotic etching chemicals are needed that can affect device performance.

Applications of silicon nanowires

It is of great interest to present applications for Si-NWs, which could benefit in unprecedented ways from both the unique and tunable properties of nanowires and the small size of these nanostructures, for use in the miniaturization of conventional devices. As the synthetic methods for the production of NWs are maturing and NWs can be made in reproducible and cost-effective ways, it is only a matter of time before applications will be explored seriously. This is a timely development, as the semiconductor industry will soon be reaching what seems to be its limit in feature-size reduction. At the same time the field of biotechnology is expanding through the availability of tremendous genome information and innovative screening assays. Since NWs are of the size of the shrinking electronic components and of cellular biomolecules, it is only natural for nanowires to be good candidates for applications in these fields.

Commercialization of NW devices, however, will require reliable mass-production, effective assembly techniques and quality-control methods. In this section, applications of nanowires to Atomic Force Microscopy (AFM), thermoelectric, and energy sector will be presented.

Production-scale fabrication method of high resolution AFM tips

It is a method of fabricating high resolution AFM tips that have a controllable diameter and a high aspect ratio [6]. The AFM is one of the foremost tools for imaging, measuring, and manipulating matter at the nanoscale level. Conventional AFM tips are fabricated by anisotropic etching of Si. These tips are formed at the end of a Si cantilever and typically have a shape of a pyramid with triangular sides defined by Si (111) surfaces. The drawback of such prior art AFM tips is their poor lateral imaging resolution due to their low aspect ratio and large radius of curvature of about 5 nm-30 nm (in the best case). The present method provides a method of fabricating high resolution AFM tips including a single semiconductor nanowire grown at an apex of a semiconductor pyramid of each AFM tip which has a controllable diameter (from 5 nm to 200 nm with additional thinning) and a high aspect ratio, e.g., length to width ratio, (on the order of greater than 100), without significant tapering from the tip of the semiconductor nanowire to its base.

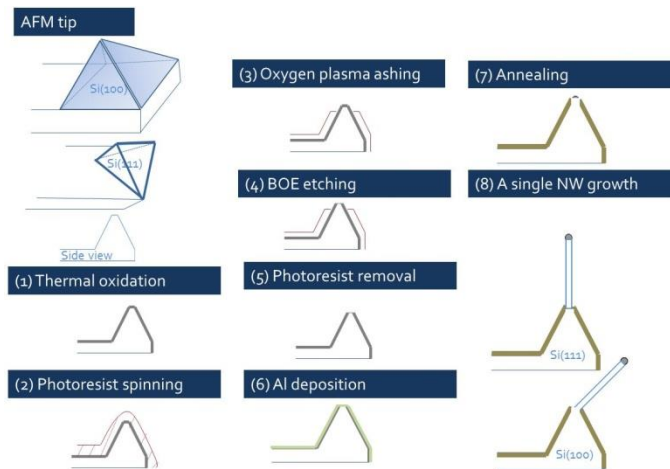


Figure 8: Schematic representations of the various steps of “Fabrication of high resolution AFM tips”.

A patterned oxide layer is formed on the AFM probe (see figure 8). The patterned oxide layer has an opening that exposes the apex of the semiconductor pyramid. A single Si-NW is grown on the exposed apex of the Si pyramid utilizing a non-oxidized Al seed material as a catalyst for NW growth. Since the single Si-NW is grown from the exposed apex of the Si pyramid, the Si-NW grows epitaxial. The Si-NW that is formed includes a p-doped Si-NW core that is surrounded by an undoped Si shell. The non-oxidized Al seed material is present at the tip of the p-doped Si-NW core. The non-oxidized Al seed material and the undoped semiconductor

shell can be removed providing a p-doped Si-NW extending from the apex of the Si pyramid.

Also, the p-doped Si-NW that is provided by the present method is stiff enough such that it can be inserted into a biological cell. Moreover, the method of the present technique can be used to tailor the dimension and the direction of the p-doped Si-NW that is produced according to specific imaging needs. Furthermore, the present method can also be employed for the mass production of AFM tips which can be easily implemented into any standard Si AFM cantilever. The method of fabrication of high resolution AFM tips is a direct application of NCT explained in the previous section and there are more applications to be built on the technique of NCT.

Photovoltaic cells based on Si-NWs

With the increasing demand for energy and the detrimental effect of fossil fuels on the environment, renewable energy sources are fast emerging as an important alternative to traditional energy sources. Among the alternatives, solar energy holds great potential due to the enormous amount of solar radiation the earth receives. It is estimated that the earth receives about 162,000 TW of solar energy every hour, which is more than 10,000 times the total worldwide energy consumption in a year even if 0.1 of the land area is covered with 10% efficient solar cells, we can meet our energy demands [42]. In addition to energy conversion, energy storage devices are also gaining increased importance due to the emergence of portable electronic devices and hybrid vehicles. Si-NWs arrays promise to reduce manufacturing costs and increase the power conversion efficiency of photovoltaic devices. In addition to better charge transport characteristics, nanowires exhibit better light harvesting properties (see figure 9).

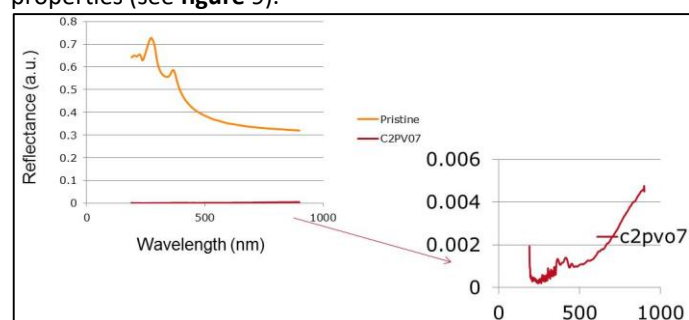


Figure 9: The reflectance of bulk Si (pristine) and Si-NWs (C2PV07). A magnified graph of the reflectance of Si-NWs shows that the reflectance is less than 0.006 (a.u.)

In figure 9 we compare the light absorption and the carrier diffusion length of thin and thick planar solar cells with a freestanding NW array solar cell. The main advantages of NWs in terms of technical performance are illustrated here. The wires create a shape that promotes scattering, thus increasing light absorption efficiencies to equivalent or better than a similarly thick planar layer. At the same time core-shell

p-n NWs structures can be grown by controlling the doping and growth parameters during and after the growth of the nanowires [43]. These core-shell PV devices allow for shorter carrier diffusion length than for planar devices of light absorptive thickness.

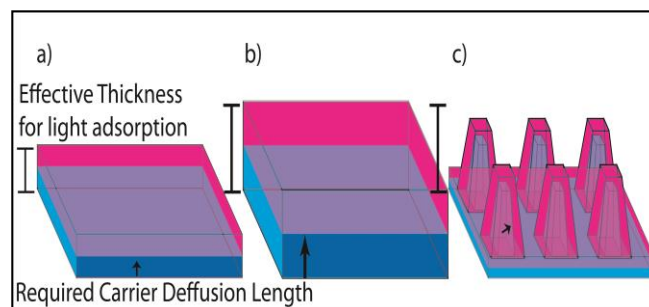


Figure 10: (a) Thin Planar Solar Cell: short carrier length, poor absorption of light. (b) Thick planar Solar Cell: long carrier diffusion length, good absorption of light. (c) Free standing nanowire solar cell: short carrier diffusion length and good absorption of light.

Photovoltaic cells based on Si-NWs exhibit lower power conversion efficiencies than conventional cells due to the enhanced photocarrier recombination associated with the nanostructures. It has been identified and separately measured surface recombination and Auger recombination in wafer-based nanostructured silicon solar cells [44]. By identifying the regimes of junction doping concentration in which each mechanism dominates, Oh and coworkers were able to design and fabricate an independently confirmed 18.2 % efficient nanostructured 'black-silicon' cell that does not need the antireflection coating layer(s) normally required to reach a comparable performance level. The results presented by Oh et al. [44] suggested design rules for efficient high-surface-area solar cells with nano- and microstructured semiconductor absorbers.

The p-n junction solar cells based on nanowires have been demonstrated in two different configurations. In the first case, the junction is radial, while in the other, the junction is planar, but with the nanowire arrays acting as an antireflecting material. Vertically aligned single crystal Si NWs were grown on a p-Type Si wafer and the excellent antireflection properties of the NWs gave conversion efficiencies of up to 9.31 % [45]. Further improvement in the efficiencies to 11.37 % was obtained for Si NW-based p-n junction solar cells by improving their antireflection properties and better electrical contact of the cells by employing slanted NW structure [46]. Their efficiencies are however; lower than the single-crystal Si solar cells in spite of higher antireflectivity due to increased carrier recombination.

A simple method has been developed [47] for creating rectifying contacts that yield photovoltaic behavior

from single Si-NWs. These devices can be used to gain insight into the performance determining properties for Si-NWs photovoltaics, such as resistivity and diffusion length, as well as the rates of bulk and surface recombination. In radial junction devices, the tradeoff between small-diameter NWs, which yield higher photovoltages due to decreased junction areas, is optimized when the wire radius is approximately equal to the minority carrier diffusion length.

All structures have a fixed wire spacing of 100 nm and wire length of 2.33 μm , but the wire diameter varies. It has been demonstrated that larger filling ratios give higher absorption at the low-frequency regime, while in the high-frequency regime NWs with smaller filling ratios, a NW structure can have overall absorption efficiency close to that of thin film. It has been demonstrated that Si-NWs have the advantages of small reflectance across a wide spectrum and can be achieved without specially designed antireflecting coatings.

Another factor in the cost is that VLS growth is inherently a vapor phase crystal growth scheme and as such must occur in a closed atmosphere controlled environment. This usually includes vacuum transfers and other procedures that can affect throughput of the samples and thus production costs negatively. This added cost to the solar cell manufacture can be mitigated somewhat by the relatively high growth rate of NWs. Compared to growing planar films, NWs grow at orders of magnitude higher growth rates in similar growth systems and parameters. This is due to the fact that vapor phase crystal growth rates are limited to some extent by volume growth rate. If one grows a continuous planar film of a certain thickness, then a given amount of growth precursors will be consumed from the vapor. On the other hand, if one consumes the same amount of precursor to grow nanowires, their height will be orders of magnitude taller than the thickness of the planar film. This is because most of the volume (between 60-90 %) between the substrate and the top of the nanowires is void, i.e. there is no crystal growing there. Thus, all the precursor material is included in the crystalline nanowires that comprise the remaining 10-40 % of the volume. In essence the much higher growth rate of the PV devices will increase the throughput to a level that will allow for lower production costs.

As mentioned earlier this void volume in the NW PV devices is not considered dead space because light scattering can allow the NW-void layer to absorb as much or more of the incoming light as an equivalently thick solid layer would absorb. This means that an equivalently thick planar layer takes much longer to grow than a NW layer. Even though the processing must include vacuum based processes that typically add higher costs due to lower throughput the higher throughput of the growth process can allow for this process to be comparably fast and thus more competitive than other planar PV vapor phase grown devices.

Microscopy and microanalysis are crucial to improving and understanding NWs growth processes and solar cell performance. The interfaces and surfaces of the nanowires and what impact they have on the solar cell device performance? These interfaces, especially the interface between the p and n areas of the solar cell diode, are critical to the quality and efficiency of solar cells. Often these interfaces are difficult to control, resulting in defects (see **figure 11**) that can affect the performance of the device.

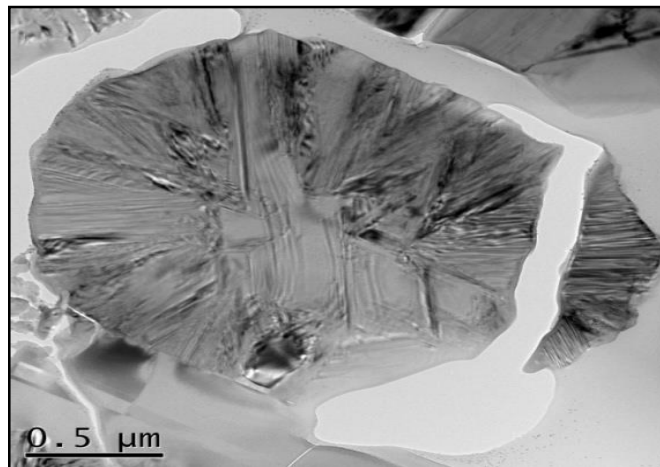


Figure 11: TEM cross section of a core-shell p-n diode nanowire, showing defects propagating from the center of the nanowire to the outside. The original wire had a diameter of ~ 50 nm and was defect free.

There is one negative aspect to using NWs in large scale PV device that is fundamental to the diode itself. The V_{oc} of any PV devices is dependent on the area of the p-n junction. The V_{oc} is defined in equation 5 where β is a constant at constant temperature, I_L is the light induced current and I_s is the dark saturation current.

$V_{oc} \equiv \frac{1}{\beta} \ln \left(\frac{I_L}{I_s} + 1 \right)$	Equation 5
--	------------

The dark saturation current is directly proportional to the area of the p-n diode. In a NW-PV device the area of the p-n diode is orders of magnitude larger than for a planar device because of the core shell structure. This means that the V_{oc} of the NW device can be lower than for a planar device. However, as mentioned above, the NW device has potentially better absorption properties and carrier collection properties which increase I_L this may not fully compensate for the large increase in I_s , but the increase I_L the I_s which makes the NW PV potentially more efficient than its' planar counterpart (see **figure 12**).

Extensive theoretical calculations predict that there are indeed parameter spaces for which the NW-PV devices outperform planar devices [8].

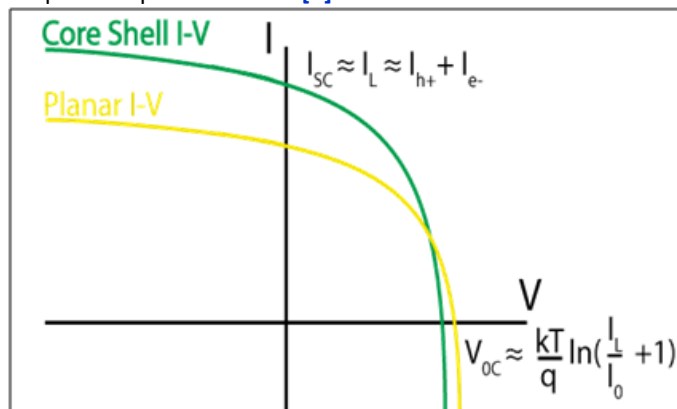


Figure 12: Illustrative comparison of I-V characteristics of planar and core-shell NW PV devices. Although the NW device has lower V_{oc} the maximum power point is higher because of the greater collection efficiency.

Thermoelectric Devices and Sensors

Thermoelectrics are devices for which a temperature gradient causes an electric current in a closed circuit, or a voltage potential in an open circuit. Using VLS grown silicon nanowires, it was established early in the lab that their thermal conductivity can be significantly reduced from the bulk value of 150 (at 300 K) to ~ 8 W/mK [33]. The size-dependent reduction in thermal conductivity is a direct result of strong phonon boundary scattering at the nanowire surface. It has been demonstrated recently that the thermal conductivity in Si-NWs can be further reduced down to almost the amorphous limit through a surface defect engineering process [9]. As a result, these rough Si-NWs behave totally differently from their bulk counterparts. At room temperature, bulk silicon is considered to be both a good thermal conductor and electron conductor, while rough Si-NWs are thermal insulators and at the same time electron conductors, making them good thermoelectric materials for waste heat recovery and power generation at a relevant temperature range.

A sensor is a device that produces some form of a measurable signal in response to an external stimulus. The properties of many materials are influenced by their surroundings. Indeed, there is a miniaturization effort in progress to reduce the size and power consumption of various analytical instruments using the advances in micro-electro-mechanical system (MEMS), and nanotechnology. Nanotechnology offers advantages with respect to some of the criteria of sensors; such as, small package, low power consumption. First, nanomaterials possess a large surface to volume ratio, leading to large adsorption rates for gases and vapors; high reactivity. These attributes of nanomaterials aid with the criteria of increased sensitivity and response.

Certainly, a reduction in size, weight, and power consumption is possible due to the small amount of active materials used in the sensor.

Future researches directions

The main practical advantage for NWs in large scale PV applications is that they can potentially be made to lower cost. One of the possible future research directions on nanotechnology is Si-NWs can be grown on cheap substrates. For example we have grown NWs on common Al foil on reusable substrates. In this process the NWs are grown on an expensive substrate that can be reused after the nanowires are removed. In both of these cases the cost of the substrate has the potential of being much less than the cost of single crystal material. The efficiency can also be almost as good or even better in some particular thickness and application range. Thus it is possible to save on the relatively high cost of the single crystal substrates and produce cells with reasonable efficiency. This may have an impact on the cost per watt production metric.

Growth of NWs on Al foil is a good illustration of how NWs can be grown, doped, and made on cheap substrates. In this case the substrate can also act as the back contact for the solar cell further enhancing the cost savings. In this case the nanowires were grown with Al as the seed similar to the procedure published earlier. A sample of ordinary Heavy Duty aluminum foil approximately 2 cm^2 was rinsed with Acetone, alcohol, and then deionized water (DI). After which it was blown dry. The substrate was then loaded into the load lock of the CVD chamber and Al was evaporated on top of the Al foil. The substrates were then transferred into the main growth chamber where they were treated at an annealing temperature of 600°C . The temperature was then lowered to 460°C and Silane (SiH_4) was introduced into the chamber. The Si-NWs subsequently grew, as it is presented in figure 13. The growth characteristics of these nanowires are similar to those grown on Si except that they are not epitaxially oriented to the substrate, which in this case was not expected because the substrate is not single crystal.

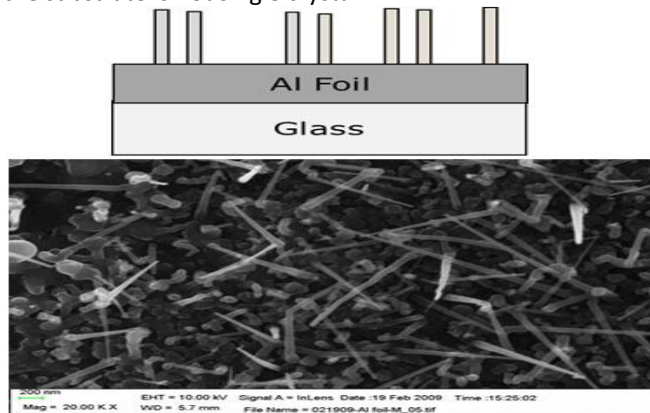


Figure 13: A schematic representation of growing Si-NWs on a cheap substrate. Nanowires grow on Al foil. Figure shows a

SEM micrograph of the grown Si-NWs on Al foil, the growth parameters are: 490 °C/ 500 mTorr SiH₄/ 30 min.

Having demonstrated that many of the most interesting discoveries to date relate to nanowire properties not present in their bulk material counterparts, we can expect future research emphasis to be increasingly focused on smaller diameter nanowires, where new unexplored physical phenomena related to quantum confinement effects are more likely to be found. We can also expect the development of applications to soon follow.

Conclusions

Epitaxial growth of Si-NWs that grows freestanding from the substrate was the topic of this article. With the remarkable progress in research on the synthesis of Si-NWs over past few years in the control growth which is accompanied by progress templating techniques. Detailed analyses have been presented of the innovative technique of NCT using oxygen reactive materials. The main advantages of NCT method are that it works for reactive seed materials that can be more desirable for many applications. This method can also have fewer steps, not requiring lift-off of a metal layer or removal of the mask. It is also amenable to standard lithography techniques as well as self-assembled patterning techniques like nanosphere lithography. Patterning and growth parameters can be chosen to achieve a high growth yield and fidelity, where no NWs grow between openings, most openings are occupied by one or more NWs and the majority is occupied by a single vertical NWs. We believe that the methodology used in achieving controlled placement of single NWs, seeded with Al is only one example of this technique and that other oxygen reactive materials such as Sn, Sb, In, Ga, and Ti and others templated by NCT will have applications in nanotechnology research as well as 3D CMOS devices (*Complementary metal-oxide-semiconductor*). The 'production scale method of high resolution AFM tips' represents a direct application of NCT technique. Nevertheless, for more applications, an improvement of current techniques of Si-NWs growth is still needed and/or an innovative technology should be developed. With the remarkable progress in research on the synthesis of Si-NWs over recent years in the control growth which is accompanied by progress templating techniques. This is highly desirable to future nano-manufacturing and applications, and is in particular an essential step towards in situ integration of well aligned Si-NWs into devices with existing technologies. The article also covered some concerns and recent demonstrations for using Si-NWs as solar cells and photonic devices.

There is no doubt that Si-NWs will create countless new opportunities and hopefully in technology. Many promising applications are now at the early demonstration stage, but are moving ahead rapidly because of their promise for new functionality, not previously available, to the fields of

electronics, optoelectronics, biotechnology, and energy conversion and generation, among others. Many exciting challenges remain in advancing both the nanoscience and then a no technological promise already demonstrated by the Si-NWs research described in this article.

REFERENCE

- [1] Li, Y., Chen, Y., Li, X., Kamins, T.I., Nauka, K. and Williams, R.S. (2004), Sequence-Specific Label-Free DNA Sensors Based on Silicon Nanowires, *Nano Lett.* 4, 245-247.
- [2] Paulo, A. S., Arellano, N., Plaza, J. A., He, R., Carraro, C., Maboudian, R., Howe, R.T., Bokor, J., Yand, P. (2007) Suspended Mechanical Structures Based on Elastic Silicon Nanowire Arrays, *Nano Lett* 7, 4, 1100-1104.
- [3] Schmidt, V., Riel, H., Senz, S., Karg, S., Riess, W. and Gosele, U. (2006) Realization of a Silicon Nanowire Vertical Surround-Gate Field-Effect Transistor, *Small* 2, 1, 85-88.
- [4] Cui, Y., Zhong, Z., Wang, D., Wang, W. and Lieber, C.M. (2003) High Performance Silicon Nanowire Field Effect Transistor, *Nano Lett.* 3, 2, 149-152.
- [5] Huo, J.; Solanki, R.; Freeouf, J. L. Carruthers (2004) J. R., Electroluminescence from silicon nanowires, *Nanotechnology* 15, 1848-1850.
- [6] Cohen, G.; Reuter, M.; Wacaser, B.; Khayyat, M.; (2012) U.S. Serial No. US 2012/0090057A1 filed on October 7, 2010 entitled "Production scale fabrication method for high resolution AFM tips".
- [7] Huang, Y.; Lieber, C. M., (2004) Integrated nanoscale electronics and optoelectronics: Exploring nanoscale science and technology through semiconductor nanowires. *Pure and Applied Chemistry*, 76 (12), 2051-2068.
- [8] Kayes, B. M.; Atwater, H. A.; Lewis, N. S., (2005) Comparison of the device physics principles of planar and radial p-n junction nanorod solar cells. *Journal of Applied Physics*, 97 (11), 114302-11.
- [9] Law, M.; Goldberger, J.; Yang, P. D., (2004) Semiconductor nanowires and nanotubes. *Annual Review of Materials Research*, 34, 83-122.
- [10] Samuelson, L.; Thelander, C.; Bjork, M. T.; Borgstrom, M.; Deppert, K.; Dick, K. A.; Hansen, A. E.; Martensson, T.; Panev, N.; Persson, A. I.; Seifert, W.; Skold, N.; Larsson, M. W.; Wallenberg, L. R., (2004) Semiconductor nanowires for 0D and 1D physics and applications. *Physica E-Low-Dimensional Systems and Nanostructures*, 25 (2-3), 313-318.
- [11] Givargizov, E. I. (1975) Fundamental aspects of VLS growth. *Journal of Crystal Growth*, 31, 20-30.
- [12] Wacaser, B. A.; Dick, K. A.; Johansson, J.; Borgström, M. T.; Deppert, K.; Lars Samuelson, (2009) Preferential Interface Nucleation: An Expansion of the VLS Growth Mechanism for Nanowires. *Advanced Materials*, 21 (2), 153-165.
- [13] Wacaser, B. A.; Reuter, M. C.; Khayyat, M. M.; Wen, C.-Y.; Haight, R.; Guha, S.; Ross, F. M., (2009) Growth System, Structure, and Doping of Aluminum-Seeded Epitaxial Silicon Nanowires. *Nano Letters*, 9 (9), 3296-3301
- [14] Wagner, R. S.; Ellis, W. C., (2010) Vapor-Liquid-Solid Mechanism of Single Crystal Growth. *Applied Physics Letters* 1964, 4 (5), 89-90.
- [15] Fan, H. J.; Werner, P.; Zacharias, M., (2006) Semiconductor Nanowires: From Self-Organization to Patterned Growth. *Small*, 2 (6), 700-717.
- [16] Kayes, M. B.; Filler, M. A.; Putnam, M. C.; Kelzenberg, M. D.; Lewis, N. S. & Atwater, H. A (2007) Growth of vertically aligned Si

wire arrays over large areas (>1 cm²) with Au and Cu catalysts, Appl. Phys. Lett. 91, 103110.

[17] Westwater, J.; Gosain, D. P.; Tomiya, S and Usui, S., (1997) Growth of silicon nanowires via gold/silane vapor-liquid-solid reaction, J. Vac. Sci. Technol. B 15(3).

[18] Westwater, J.; Gosain, D. P.; Usui, S., (1997) Control of the Size and Position of Silicon Nanowires Grown via the Vapor-Liquid-Solid Technique. Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers, 36 (10), 6204-6209.

[19] Renard, V. T.; Jublot, M.; Gergaud, P.; Cherns, P.; Rouchon, D.; Chabli, A.; Jousseau, V., (2009) Catalyst preparation for CMOS-compatible silicon nanowire synthesis. Nat Nano, 4 (10), 654-657.

[20] Whang, S.; Lee, S.; Chi, D.; Yang, W.; Cho, B.; Liew, Y. and Kwong, D. (2007) B-doping of vapour-liquid-solid grown Au-catalysed and Al-catalysed Si nanowires: effects of B₂H₆ gas during Si nanowires growth and B-doping by a post-synthesis in situ plasma process, Nanotechnology 18 275302, pp 1-4.

[21] Ke, Y.; Weng, X.; Redwing, J. M.; Eichfeld, C. M.; Swisher, T. R.; Mohney, S. E.; Habib, Y. M., (2009) Fabrication and Electrical Properties of Si Nanowires Synthesized by Al Catalyzed Vapor-Liquid-Solid Growth. Nano Letters, 9 (12), 4494-4499.

[22] Chaudhari, P.; Shim, H.; Wacaser, B. A.; Reuter, M. C.; Murray, C.; Reuter, K. B.; Jordan-Sweet, J.; Ross, F. M.; Guha, S., (2010) Heteroepitaxial silicon film growth at 600 °C from an Al-Si eutectic melt. Thin Solid Films, 518 (19), 5368-5371.

[23] Tutuc, E.; Guha, S.; Chu, J. O., (2006) Morphology of germanium nanowires grown in presence of B₂H₆. Applied Physics Letters, 88 (4), 043113-3.

[24] Roberts, S.; Dobson, P. J., (1981) Evidence for reaction at the Al-SiO₂ interface. Journal of Physics D: Applied Physics, 14 (3), L17.

[25] Krug, C.; da Rosa, E. B. O.; de Almeida, R. M. C.; Morais, J.; Baumvol, I. J. R.; Salgado, T. D. M.; Stedile, F. C., Atomic Transport and Chemical Stability during Annealing of Ultrathin Al₂O₃ Films on Si. Physical Review Letters 2000, 85 (19), 4120

[26] Wang, K.; Gunawan, O.; Moumen, N.; Tulevski, G.; Mohamed, H.; Fallah, B.; Tutuc, E.; Guha, S., Wire-textured silicon solar cells, IEEE Proceedings PVSC 2010, 35, 000913 - 000917.

[27] Lauhon, L., Gudisen, M. and Lieber, C. (2004) Semiconductor nanowire heterostructures Philosophical Transactions of the Royal Society of London. Series A 362, 1247-1260.

[28] Bootsma, G. A. and Gassen, H.J. (1971) A quantitative study on the growth of silicon whiskers from silane and germanium whiskers from germane. Journal of Crystal Growth 10, 223-234.

[29] Kamins, T. I.; Williams, R. S.; Basile, D. P.; Hesjedal, T.; Harris, J. S., (2001) Ti-catalyzed Si nanowires by chemical vapor deposition: Microscopy and growth mechanisms. Journal of Applied Physics, 89 (2), 1008-1016.

[30] Persson, A. I., Larsson, M.W., Stenstrom, S., Ohlsson, B. J., Samuelson, L. & Wallenberg, L. R. (2004) Solid-phase diffusion mechanism for GaAs nanowire growth. Nature Materials 3, 677-681.

[31] Trentler, T. J., Hickman, K. M., Goel, S. C., Viano, A. M., Gibbons, P. C. and Buhro, W. E. (1995) Solution-Liquid-Solid Growth of Crystalline III-V Semiconductors: An Analogy to Vapor-Liquid-Solid Growth. Science 270, 1791-1794.

[32] Fang, Y. P., Wen, X. G. & Yang, (2006) S. H. Hollow and tin-filled nanotubes of single-crystalline In(OH)₃ grown by a solution-liquid-solid-solid route. Angewandte Chemie-International Edition 45, 4655-4658.

[33] Zhang, L. Li, Y.; Li, G. and Zhang, L. (2003), Chem. Phys. Lett. 378, 244.

[34] Tian, M. ; Wang, J. ; Kumar, N. ; Han, T. ; Kobayashi, Y. ; Liu, Y. ; Mallouk, T.E. ; and Chen, M.H.W. (2006) Nano Lett., 6,2773.

[35] Civale, Y.; Nanver, L. K.; Hadley, P.; Goudena, E. J. G.; Schellevis, H., (2006) Sub-500°C solid-phase epitaxy of ultra-abrupt p+-silicon elevated contacts and diodes. IEEE Electron Device Letters, 27, 341-343.

[36] Givargizov, E. I. (1975) Fundamental aspects of VLS growth. Journal of Crystal Growth, 31, 20-30.

[37] Hutchby, J.; Bourianoff, G.I.; Zhirnov, V.V. and Brewer, J.E. (2002) IEEE Cir Dev. 28.

[38] Johansson, J. ;Wacaser, B.A. ; Dick, K.A. ; and Seifert, W. (2006) Nanotechnology 17, S355.

[39] Meyyappan, M; and Sunkara, M. K. (2010) Inorganic nanowires: Applications properties and characterization, Taylor and Francis group, LLC, USA.

[40] Guichard, A. R.; Barsic, D.N.; Sharma, S.; Kamins, T.I. and Brongersma, M.L. (2006) Nano Lett. 6, 2140.

[41] Baron, T.; Gordon, M.; Dhalluin, F.; TERNON, C.; Ferret, P.; and Gentile, P. (2006) Appl. Phys. Lett. 80, 23311.

[42] US Department of Energy (2005) Basic Research Needs for Solar Energy Utilization, Report of the Basic Energy Sciences Workshop on Solar Energy Utilization, Published by the Office of Science.

[43] Kelzenberg, M. D.; Boettcher, S. W. ; Petykiewicz, J. A. ; Turner-Evans, D. B. ; Putnam, M. C. ; Warren, E. L. ; Spurgeon, J. M. ; Briggs, R. M. ; Lewis, N. S. and Atwater, H. A. (2010) Nature Materials, Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications, p.1-5.

[44] Oh, J.; Yuan, H. and Branz, H. (2012) An 18.2%-efficient black-silicon solar cell achieved through control of carrier recombination in nanostructures, Nature Nanotechnology, Advance Online Publication 1-6.

[45] Peng, K.; Xu, Y.; Wu, Y.; Yan, Y.; Lee, S. T. and Zhu, J. (2005) small 1, 1062.

[46] Hui, F.; Xudong, L.; Shuang, S.; Ying, X. and Jing, Z. (2008) Nanotechnology 19, 255703.

[47] Kelzenberg, M. D.; Turner-Evans, D. B.; Kayes, B. M.; Filler, Putnam, M. C.; Lewis, N. S. & Atwater, H. A. (2008) Photovoltaic Measurements in Single-Nanowire Silicon Solar Cells, Nano Lett. 8, 2, 710-714.